WHAT IS CLAIMED IS:

1. An array of non-volatile memory cells comprising:

a semiconductor substrate;

a plurality of non-volatile memory cells formed in said substrate, arranged in a plurality of rows and columns;

each memory cell comprising;

a first terminal and a second terminal with a channel therebetween in said substrate, said channel having a first portion and a second portion;

a transistor gate insulated from said substrate and positioned to control the conduction of current in said first portion of said channel;

a floating gate insulated from said substrate and positioned to control the conduction of current in said second portion of said channel;

a control gate capacitively coupled to the floating gate;

a plurality of buried bit lines in said substrate arranged substantially parallel to one another;

each buried bit line electrically connected to the first terminal of memory cells arranged in the same column; wherein adjacent memory cells in the same row share a common buried bit line;

a plurality of buried source lines in said substrate arranged substantially parallel to one another; each buried source line electrically connected to the second terminal of memory cells arranged in the same column; wherein adjacent memory cells in the same row share a common buried source line;

a plurality of gate lines arranged substantially parallel to one another, each gate line electrically connected to the transistor gate of memory cells arranged in the same column; and

a plurality of word lines arranged substantively parallel to one another, each word line electrically connected to the control gate of memory cells arranged in the same row.

2. The array of claim 1 wherein said first portion of said channel is adjacent to said first terminal, and said second portion of said channel is adjacent to and between said first portion of said channel and said second terminal and wherein said buried bit line is between adjacent

transistor gates of cells adjacent to one another in the same row; and wherein said buried source line is between adjacent floating gates of cells adjacent to one another in the same row.

3. The array of claim 2 further comprising;

a plurality of trenches in said substrate substantially parallel to one another; each trench having a first sidewall, a second sidewall and a bottom wall;

each buried source line being along said bottom wall of a trench;

wherein floating gates of first memory cells in the same column are positioned in the same trench insulated from said first sidewall, and floating gates of second memory cells in the same column, adjacent to said first memory cells are positioned in said same trench insulated from said second sidewall.

4. The array of claim 3 wherein adjacent memory cells in the same row share a common control gate and wherein said common control gate is positioned in said trench insulated from said floating gates.

5. The array of claim 4 wherein said plurality of trenches are spaced apart from one another, with a substantially planar surface on said substrate between each pair of adjacent trenches; wherein transistor gates of memory cells, are insulated and spaced apart from the planar surface, and each transistor gate is adjacent to a trench.

6. The array of claim 5 wherein each of said buried bit lines is in said substrate along said planar surface and between a pair of transistor gates.

7. The array of claim 2 further comprising;

a plurality of trenches in said substrate substantially parallel to one another; each trench having a first sidewall, a second sidewall and a bottom wall;

each buried bit line being along said bottom wall of a trench;

wherein transistor gates of first memory cells in the same column are positioned in the same trench insulated from said first sidewall, and transistor gates of second memory cells

in the same column, adjacent to said first memory cells are positioned in said same trench insulated from said second sidewall.

8. The array of claim 7 wherein adjacent memory cells in the same row share a common transistor gate and wherein said common transistor gate is positioned in said trench insulated from said first and second side walls.

9. The array of claim 8 wherein said plurality of trenches are spaced apart from one another, with a substantially planar surface on said substrate between each pair of adjacent trenches; wherein floating gates of memory cells, are insulated and spaced apart from the planar surface, and each floating gate is adjacent to a trench.

10. The array of claim 9 wherein each of said buried source lines is in said substrate along said planar surface and between a pair of floating gates.

11. A method of erasing a selected non-volatile memory cell in an array having a plurality of non-volatile memory cells formed in a semiconductor substrate, arranged in a plurality of rows and columns; a plurality of trenches in said substrate substantially parallel to one another; each trench having a sidewall, and a bottom wall; wherein each memory cell comprising a first terminal and a second terminal with a channel therebetween in said substrate, said channel having a first portion and a second portion; a transistor gate insulated from said substrate and positioned to control the conduction of current in said first portion of said channel; a floating gate in a trench insulated from said substrate and positioned to control the conduction of current in said second portion of said channel, along said sidewall of said trench; a control gate in the same trench capacitively coupled to the floating gate; a plurality of buried bit lines in said substrate arranged substantially parallel to one another; each buried bit line electrically connected to the first terminal of memory cells arranged in the same column; wherein adjacent memory cells in the same row share a common buried bit line; a plurality of buried source lines in said substrate arranged substantially parallel to one another; each buried source line electrically connected to the second terminal of memory cells arranged in the same column, each second terminal being in the substrate in the bottom wall of a trench; wherein adjacent memory

cells in the same row share a common buried source line; a plurality of gate lines arranged substantially parallel to one another, each gate line electrically connected to the transistor gate of memory cells arranged in the same column; and a plurality of word lines arranged substantively parallel to one another, each word line electrically connected to the control gate of memory cells arranged in the same row, said method comprising;

applying a first positive voltage to a word line connected to a control gate of said selected memory cell;

applying a second voltage to a gate line connected to a transistor gate of said selected memory cell;

applying a third voltage to a buried bit line connected to a first terminal of said selected memory cell;

applying a fourth voltage to a buried source line connected to a second terminal of said selected memory cell;

wherein said first positive voltage is more positive than said second voltage, third voltage or fourth voltage;

whereby electrons from said floating gate of said selected memory cell tunnel to said control gate of said selected memory cell thereby erasing the floating gate.

12. The method of claim 11 wherein said second voltage, third voltage and fourth voltage are all ground.

13. The method of claim 12 further comprising

applying a ground voltage to the word lines which are not connected to the control gates of the selected memory cell.

14. A method of erasing a selected non-volatile memory cell in an array having a plurality of non-volatile memory cells formed in a semiconductor substrate, arranged in a plurality of rows and columns; a plurality of trenches in said substrate substantially parallel to one another; each trench having a sidewall, and a bottom wall; wherein each memory cell comprising a first terminal and a second terminal with a channel therebetween in said substrate, said channel having a first portion and a second portion; a transistor gate insulated from said substrate and

positioned to control the conduction of current in said first portion of said channel; a floating gate in a trench insulated from said substrate and positioned to control the conduction of current in said second portion of said channel, along said sidewall of said trench; a control gate in the same trench capacitively coupled to the floating gate; a plurality of buried bit lines in said substrate arranged substantially parallel to one another; each buried bit line electrically connected to the first terminal of memory cells arranged in the same column; wherein adjacent memory cells in the same row share a common buried bit line; a plurality of buried source lines in said substrate arranged substantially parallel to one another; each buried source line electrically connected to the second terminal of memory cells arranged in the same column, each second terminal being in the substrate in the bottom wall of a trench; wherein adjacent memory cells in the same row share a common buried source line; a plurality of gate lines arranged substantially parallel to one another, each gate line electrically connected to the transistor gate of memory cells arranged in the same column; and a plurality of word lines arranged substantively parallel to one another, each word line electrically connected to the control gate of memory cells arranged in the same row, said method comprising;

applying a negative voltage to a word line connected to a control gate of a selected memory cell;

applying a positive voltage to a gate line connected to the transistor gate of a selected memory cell;

applying a first voltage to a buried bit line connected to a first terminal of a selected memory cell;

applying a second voltage to a buried source line connected to a second terminal of a selected memory cell;

whereby electrons from said floating gate tunnel to said transistor gate thereby erasing the floating gate.

15. The method of claim 14 wherein said first and second voltages are ground.

16. The method of claim 14 further comprising reading said selected memory cell, and applying a non-positive voltage to said gate line connected to the transistor gate of the selected memory cell, in the event the selected memory cell is erased.

17. The method of claim 16 wherein said selected memory cell is iteratively erased, and read, with the voltage applied to the gate line connected to the transistor gate of the selected memory cell used to control the cessation of the erase cycle.

18. A method of erasing a selected non-volatile memory cell in an array having a plurality of non-volatile memory cells formed in a semiconductor substrate, arranged in a plurality of rows and columns; a plurality of trenches in said substrate substantially parallel to one another; each trench having a sidewall, and a bottom wall; wherein each memory cell comprising a first terminal and a second terminal with a channel therebetween in said substrate, said channel having a first portion and a second portion; a transistor gate insulated from said substrate and positioned to control the conduction of current in said first portion of said channel; a floating gate in a trench insulated from said substrate and positioned to control the conduction of current in said second portion of said channel, along said sidewall of said trench; a control gate in the same trench capacitively coupled to the floating gate; a plurality of buried bit lines in said substrate arranged substantially parallel to one another; each buried bit line electrically connected to the first terminal of memory cells arranged in the same column; wherein adjacent memory cells in the same row share a common buried bit line; a plurality of buried source lines in said substrate arranged substantially parallel to one another; each buried source line electrically connected to the second terminal of memory cells arranged in the same column, each second terminal being in the substrate in the bottom wall of a trench; wherein adjacent memory cells in the same row share a common buried source line; a plurality of gate lines arranged substantially parallel to one another, each gate line electrically connected to the transistor gate of memory cells arranged in the same column; and a plurality of word lines arranged substantively parallel to one another, each word line electrically connected to the control gate of memory cells arranged in the same row, said method comprising;

applying a negative voltage to a word line connected to a control gate of a

selected memory cell;

applying a first voltage to a gate line connected to the transistor gate of a selected memory cell;

applying a positive voltage to a buried source line connected to a second terminal of a selected memory cell;

whereby electrons from said floating gate tunnel to said source line thereby erasing the floating gate.

19. The method of claim 18 wherein said first voltage is ground.

20. The method of claim 19 further comprising applying a ground voltage to the word lines not connected to the control gate of the selected memory cell.

21. The method of claim 18 wherein said method erases a pair of adjacently positioned memory cells each having a floating gate in a common trench with a source line in common.

22. A method of making an isolation-less array of non-volatile memory cells in a semiconductor substrate of a first conductively type comprising;

forming a plurality of spaced apart trenches in said substrate in a first direction, each trench having a first sidewall, a second sidewall and a bottom wall;

forming a first terminal of a second conductivity type along the bottom wall of each trench in the substrate;

forming a pair of floating gates along the first and second sidewalls in each trench, each floating gate spaced apart from the first and second sidewalls, respectively;

forming a control gate in each trench; each control gate insulated from and capacitively coupled to the floating gates in the trench and insulated from the first terminal along the bottom wall of the trench;

patterning said substrate along a second direction substantially perpendicular to said first direction and forming a plurality of spaced apart insulation regions in each trench and forming a plurality of floating gates in said first direction insulated from one another;

forming a plurality of spaced apart, substantially parallel, transistor gates, each

transistor gate extending in said first direction and spaced apart and insulated from the substrate, and positioned adjacent to a trench in a region between each pair of trenches;

forming a second terminal of the second conductively type extending in said first direction in the substrate, between each pair of transistor gates in a region between each pair of trenches; and

forming an electrical contact to each control gate in the same second direction.

23. A method of making an isolation-less array of non-volatile memory cells in a semiconductor substrate of a first conductively type, comprising;

forming a plurality of spaced apart substantially parallel masked regions on said substrate in a first direction, wherein an unmasked region is formed on said substrate between each pair of adjacent masked regions;

forming a pair of spaced apart transistor gates substantially parallel to one another extending in said first direction in each unmasked region, with each transistor gate adjacent to a masked region, spaced apart and insulated from the substrate;

forming a first terminal of a second conductively type in said substrate, extending in said first direction, between each pair of transistor gates in each unmasked region;

removing said masked regions;

forming a trench region in said substrate extending in said first direction, between each pair of adjacent unmasked regions; each trench having a first sidewall, a second sidewall, and a bottom wall;

forming a second terminal of a second conductively type in the substrate extending in said first direction, along the bottom wall of each trench;

forming a pair of floating gates along the first and second sidewalls, respectively, in each trench, each floating gate spaced apart from its respective sidewall;

forming a control gate in each trench; each control gate insulated from and capacitively coupled to the floating gates in the trench and insulated from the second terminal along the bottom wall of each trench;

patterning each trench along a second direction substantially perpendicular to said first direction and forming a plurality of spaced apart insulation regions in each trench; and

forming an electrical contact to each control gate that are positioned in the same second direction.

24. An array of non-volatile memory cells comprising:

a semiconductor substrate;

a plurality of non-volatile memory cells formed in said substrate, arranged in a plurality of rows and columns;

each memory cell comprising;

a first terminal and a second terminal with a channel therebetween in said substrate;

a trench extending in a column direction in said substrate, said trench having a sidewall and a bottom wall;

a floating gate in said trench and insulated from said sidewall positioned to control the conduction of current in said channel;

a control gate in said trench capacitively coupled to the floating gate;

said first terminal in said substrate along the bottom wall of said trench;

said second terminal in said substrate and adjacent to said trench;

a plurality of buried bit lines in said substrate arranged substantially parallel to one another;

each buried bit line electrically connected to the second terminal of memory cells arranged in the same column; wherein adjacent memory cells in the same row share a common buried bit line;

a plurality of buried source lines in said substrate arranged substantially parallel to one another; each buried source line electrically connected to the first terminal of memory cells arranged in the same column; wherein adjacent memory cells in the same row share a common buried source line;

a plurality of word lines arranged substantively parallel to one another, each word line electrically connected to the control gate of memory cells arranged in the same row.

25. The array of claim 24 wherein said buried bit line is between adjacent trenches of cells adjacent to one another in the same row; and wherein said buried source line is between adjacent floating gates of cells adjacent to one another in the same row.

26. The array of claim 25 further comprising;

each trench having a first sidewall, a second sidewall and a bottom wall;

wherein floating gates of first memory cells in the same column are positioned in the same trench insulated from said first sidewall, and floating gates of second memory cells in the same column, adjacent to said first memory cells are positioned in said same trench insulated from said second sidewall.

27. The array of claim 26 wherein adjacent memory cells in the same row share a common control gate and wherein said common control gate is positioned in said trench insulated from said floating gates.

28. An array of bi-directional non-volatile memory cells comprising:

a semiconductor substrate;

a plurality of non-volatile memory cells formed in said substrate, arranged in a plurality of rows and columns;

each memory cell comprising;

a first terminal and a second terminal with a channel therebetween in said substrate, said channel having a first portion, a second portion, and a third portion;

a transistor gate insulated from said substrate and positioned to control the conduction of current in said second portion of said channel;

a first floating gate insulated from said substrate and positioned to control the conduction of current in said first portion of said channel;

a second floating gate insulated from said substrate and positioned to control the conduction of current in said third portion of said channel;

said second portion between said first portion and said third portion;

a first control gate capacitively coupled to the first floating gate;

a second control gate capacitively coupled to the second floating gate;

a plurality of buried bit lines in said substrate arranged substantially parallel to one another and arranged to connect memory cells in the same column;

each of a first plurality of buried bit lines is electrically connected to the first terminal of memory cells arranged in the same column; wherein adjacent memory cells in the same row share a common first terminal;

each of a second plurality of buried bit line is electrically connected to the second terminal of memory cells arranged in the same column, wherein adjacent memory cells in the same row share a common second terminal;

a plurality of gate lines arranged substantially parallel to one another, each gate line electrically connected to the transistor gate of memory cells arranged in the same column; and

a plurality of word lines arranged substantially parallel to one another, each word line electrically connected to the first and second control gates of each memory cell arranged in the same row.

29. The array of claim 28 further comprising;

a plurality of spaced apart trenches in said substrate substantially parallel to one another; each trench having a first sidewall, a second sidewall and a bottom wall, with a planar portion of said substrate between each adjacent trench;

each of said first and second buried bit lines being along said bottom wall of a trench;

wherein first floating gates of first memory cells in the same column are positioned in the same trench insulated from said first sidewall, and first floating gates of second memory cells in the same column, adjacent to said first memory cells are positioned in said same trench insulated from said second sidewall.

30. The array of claim 29 wherein adjacent memory cells in the same row to one side share a common first control gate and wherein said common first control gate is positioned in said trench insulated from said floating gates.

31. The array of claim 30 wherein adjacent memory cells in the same row to another side share a common second control gate and wherein said common second control gate is positioned in said trench insulated from said floating gates.

32. The array of claim 29 wherein said plurality of trenches are spaced apart from one another, with a substantially planar surface on said substrate between each pair of adjacent trenches; wherein the transistor gate of memory cells, are insulated and spaced apart from the planar surface.

33. The array of claim 28 further comprising;

a plurality of spaced apart trenches in said substrate substantially parallel to one another; each trench having a first sidewall, a second sidewall and a bottom wall, with a planar portion of said substrate between each adjacent trench;

each first and second buried bit line being along said planar portion of said substrate between each adjacent trench;

wherein first floating gates of first memory cells in the same column are spaced apart from said planar portion of said substrate between a first buried bit line and a trench to one side, and first floating gates of second memory cells in the same column, adjacent to said first memory cells are spaced apart from said planar portion of said substrate between a second buried bit line and a trench to another side.

34. The array of claim 33 wherein the transistor gate of a memory cell is in a trench spaced apart from the first and second side walls.

35. The array of claim 34 wherein adjacent memory cells in the same row to one side share a common first control gate and wherein said common first control gate is capacitively coupled to said first floating gates of said first and second memory cells.

36. The array of claim 35 wherein adjacent memory cells in the same row to another side share a common second control gate and wherein said common second control gate is capacitively coupled to said second floating gates of said first and second memory cells.

37. A method of erasing a selected non-volatile memory cell in an array of bi-directional non-volatile memory cells formed in a semiconductor substrate having a plurality of non-volatile memory cells formed in said substrate, arranged in a plurality of rows and columns; a plurality of spaced apart trenches in said substrate substantially parallel to one another; each trench having a first sidewall, a second sidewall and a bottom wall, with a planar portion of said substrate between each adjacent trench; with each memory cell comprising a first terminal and a second terminal with a channel therebetween in said substrate, said channel having a first portion, a second portion, and a third portion; said first portion being along a first sidewall of a first trench, said third portion being along a second sidewall of a second trench, and said second portion being along said planar portion between said first and second trenches; a transistor gate insulated from said planar portion of said substrate and positioned to control the conduction of current in said second portion of said channel; a first floating gate insulated from said substrate and positioned to control the conduction of current in said first portion of said channel; a second floating gate insulated from said substrate and positioned to control the conduction of current in said third portion of said channel; a first control gate capacitively coupled to the first floating gate; a second control gate capacitively coupled to the second floating gate; a plurality of buried bit lines in said substrate arranged substantially parallel to one another and arranged to connect memory cells in the same column; each first buried bit line electrically connected to the first terminal of memory cells arranged in the same column; wherein adjacent memory cells in the same row share a common first terminal; said first terminal being along the bottom wall of said first trench; each second buried bit line electrically connected to the second terminal of memory cells arranged in the same column, wherein adjacent memory cells in the same row share a common second terminal; said second terminal being along the bottom wall of said second trench; a plurality of gate lines arranged substantially parallel to one another, each gate line electrically connected to the transistor gate of memory cells arranged in the same column; and a plurality of word lines arranged substantively parallel to one another, each word line electrically connected to the first and second control gates of each memory cell arranged in the same row; wherein first floating gates of first memory cells in the same column are positioned in the same trench insulated from said first sidewall, and first floating gates of second memory cells in the same column, adjacent to said first memory cells are positioned in said same trench insulated

from said second sidewall; said method comprising;

applying a first positive voltage to a word line connected to the first and second control gates of the selected memory cell;

applying a second voltage to a gate line connected to the transistor gate of the selected memory cell;

applying a third voltage to a first buried bit line connected to a first terminal of the selected memory cell;

applying a fourth voltage to a second buried bit line connected to a second terminal of the selected memory cell;

wherein said first positive voltage is more positive than said second voltage, third voltage or fourth voltage;

whereby electrons from said first and second floating gates of said selected memory cell tunnel to said first and second control gates, respectively of said selected memory cell thereby erasing the floating gate.

38. The method of claim 37 wherein said second voltage, third voltage and fourth voltage are all ground.

39. The method of claim 38 further comprising

applying a ground voltage to the word lines which are not connected to the first and second control gates of the selected memory cell.

40. A method of erasing a selected non-volatile memory cell in an array of bi-directional non-volatile memory cells formed in a semiconductor substrate having a plurality of non-volatile memory cells formed in said substrate, arranged in a plurality of rows and columns; a plurality of spaced apart trenches in said substrate substantially parallel to one another; each trench having a first sidewall, a second sidewall and a bottom wall, with a planar portion of said substrate between each adjacent trench; with each memory cell comprising a first terminal and a second terminal with a channel therebetween in said substrate, said channel having a first portion, a second portion, and a third portion; said first portion being along a first sidewall of a first trench, said third portion being along a second sidewall of a second trench, and said second portion

being along said planar portion between said first and second trenches; a transistor gate insulated from said planar portion of said substrate and positioned to control the conduction of current in said second portion of said channel; a first floating gate insulated from said substrate and positioned to control the conduction of current in said first portion of said channel; a second floating gate insulated from said substrate and positioned to control the conduction of current in said third portion of said channel; a first control gate capacitively coupled to the first floating gate; a second control gate capacitively coupled to the second floating gate; a plurality of buried bit lines in said substrate arranged substantially parallel to one another and arranged to connect memory cells in the same column; each first buried bit line electrically connected to the first terminal of memory cells arranged in the same column; wherein adjacent memory cells in the same row share a common first terminal; said first terminal being along the bottom wall of said first trench; each second buried bit line electrically connected to the second terminal of memory cells arranged in the same column, wherein adjacent memory cells in the same row share a common second terminal; said second terminal being along the bottom wall of said second trench; a plurality of gate lines arranged substantially parallel to one another, each gate line electrically connected to the transistor gate of memory cells arranged in the same column; and a plurality of word lines arranged substantively parallel to one another, each word line electrically connected to the first and second control gates of each memory cell arranged in the same row; wherein first floating gates of first memory cells in the same column are positioned in the same trench insulated from said first sidewall, and first floating gates of second memory cells in the same column, adjacent to said first memory cells are positioned in said same trench insulated from said second sidewall; said method comprising;

applying a negative voltage to a word line connected to the first and second control gates of a selected memory cell;

applying a positive voltage to a gate line connected to the transistor gate of the selected memory cell;

applying a first voltage to a first buried bit line connected to a first terminal of the selected memory cell;

applying a second voltage to a second buried bit line connected to a second terminal of the selected memory cell;

whereby electrons from said first and second floating gates tunnel to said transistor gate thereby erasing the floating gate.

41. The method of claim 40 wherein said first and second voltages are ground.

42. The method of claim 40 further comprising reading said selected memory cell, and applying a non-positive voltage to said gate line connected to the transistor gate of the selected memory cell, in the event the selected memory cell is erased.

43. The method of claim 42 wherein said selected memory cell is iteratively erased, and read, with the voltage applied to the gate line connected to the transistor gate of the selected memory cell used to control the cessation of the erase cycle.

44. A method of erasing a selected non-volatile memory cell in an array of bi-directional non-volatile memory cells formed in a semiconductor substrate having a plurality of non-volatile memory cells formed in said substrate, arranged in a plurality of rows and columns; a plurality of spaced apart trenches in said substrate substantially parallel to one another; each trench having a first sidewall, a second sidewall and a bottom wall, with a planar portion of said substrate between each adjacent trench; with each memory cell comprising a first terminal and a second terminal with a channel therebetween in said substrate, said channel having a first portion, a second portion, and a third portion; said first portion being along a first sidewall of a first trench, said third portion being along a second sidewall of a second trench, and said second portion being along said planar portion between said first and second trenches; a transistor gate insulated from said planar portion of said substrate and positioned to control the conduction of current in said second portion of said channel; a first floating gate insulated from said substrate and positioned to control the conduction of current in said first portion of said channel; a second floating gate insulated from said substrate and positioned to control the conduction of current in said third portion of said channel; a first control gate capacitively coupled to the first floating gate; a second control gate capacitively coupled to the second floating gate; a plurality of buried bit lines in said substrate arranged substantially parallel to one another and arranged to connect memory cells in the same column; each first buried bit line electrically connected to the first

terminal of memory cells arranged in the same column; wherein adjacent memory cells in the same row share a common first terminal; said first terminal being along the bottom wall of said first trench; each second buried bit line electrically connected to the second terminal of memory cells arranged in the same column, wherein adjacent memory cells in the same row share a common second terminal; said second terminal being along the bottom wall of said second trench; a plurality of gate lines arranged substantially parallel to one another, each gate line electrically connected to the transistor gate of memory cells arranged in the same column; and a plurality of word lines arranged substantively parallel to one another, each word line electrically connected to the first and second control gates of each memory cell arranged in the same row; wherein first floating gates of first memory cells in the same column are positioned in the same trench insulated from said first sidewall, and first floating gates of second memory cells in the same column, adjacent to said first memory cells are positioned in said same trench insulated from said second sidewall; said method comprising;

applying a negative voltage to a word line connected to the first and second control gates of a selected memory cell;

applying a first voltage to a gate line connected to the transistor gate of the selected memory cell;

applying a positive voltage to a second buried bit line connected to a second terminal of the selected memory cell;

whereby electrons from said second floating gate tunnel to said second buried bit line thereby erasing the second floating gate.

45. The method of claim 44 wherein said first voltage is ground.

46. The method of claim 45 further comprising applying a ground voltage to the word lines not connected to the control gates of the selected memory cell.

47. The method of claim 44 further comprising;

applying a positive voltage to a first buried bit line connected to a first terminal of the selected memory cell;

whereby electrons from said first floating gate tunnel to said first buried bit line thereby erasing the first floating gate.

48. A method of reading a selected non-volatile memory cell in an array of bi-directional non-volatile memory cells formed in a semiconductor substrate; having a plurality of non-volatile memory cells formed in said substrate, arranged in a plurality of rows and columns; with each memory cell comprising; a first terminal and a second terminal with a channel therebetween in said substrate, said channel having a first portion, a second portion, and a third portion; a transistor gate insulated from said substrate and positioned to control the conduction of current in said second portion of said channel; a first floating gate insulated from said substrate and positioned to control the conduction of current in said first portion of said channel; a second floating gate insulated from said substrate and positioned to control the conduction of current in said third portion of said channel; said second portion between said first portion and said third portion; a first control gate capacitively coupled to the first floating gate; a second control gate capacitively coupled to the second floating gate; a plurality of buried bit lines in said substrate arranged substantially parallel to one another and arranged to connect memory cells in the same column; each first buried bit line electrically connected to the first terminal of memory cells arranged in the same column; wherein adjacent memory cells in the same row share a common first terminal; each second buried bit line electrically connected to the second terminal of memory cells arranged in the same column, wherein adjacent memory cells in the same row share a common second terminal; a plurality of gate lines arranged substantially parallel to one another, each gate line electrically connected to the transistor gate of memory cells arranged in the same column; and a plurality of word lines arranged substantively parallel to one another, each word line electrically connected to the first and second control gates of each memory cell arranged in the same row; said method comprising;

applying a first positive voltage to a second buried bit line connecting the second terminal of the selected memory cell;

applying a second positive voltage to a word line connecting to the first and second control gates of the selected memory cell sufficient t o turn on said first and third portions of said the channel of the selected memory cell irrespective of the charges stored on the first and second

floating gates; and

applying a third positive voltage to the transistor gate of the selected memory cell;

whereby the current through the first portion of the channel is a function of the charges stored on the first floating gate of the selected memory cell and a voltage equal to said third positive voltage minus the voltage drop across the threshold of the second portion of the channel of the selected memory cell.

49. The method of claim 48 wherein a fourth voltage, insufficient to turn on the second portion of the channel is supplied to memory cells in unselected columns of said array.

50. The method of claim 49 wherein a fifth voltage insufficient to turn on the first and second portions of the channel is supplied to memory cells in unselected rows of said array.

51. A method of programming a selected non-volatile memory cell in an array of bi-directional non-volatile memory cells formed in a semiconductor substrate having a plurality of non-volatile memory cells formed in said substrate, arranged in a plurality of rows and columns; a plurality of spaced apart trenches in said substrate substantially parallel to one another; each trench having a first sidewall, a second sidewall and a bottom wall, with a planar portion of said substrate between each adjacent trench; with each memory cell comprising a first terminal and a second terminal with a channel therebetween in said substrate, said channel having a first portion, a second portion, and a third portion; said first portion being along a first sidewall of a first trench, said third portion being along a second sidewall of a second trench, and said second portion being along said planar portion between said first and second trenches; a transistor gate insulated from said planar portion of said substrate and positioned to control the conduction of current in said second portion of said channel; a first floating gate insulated from said substrate and positioned to control the conduction of current in said first portion of said channel; a second floating gate insulated from said substrate and positioned to control the conduction of current in said third portion of said channel; a first control gate capacitively coupled to the first floating gate; a second control gate capacitively coupled to the second floating gate; a plurality of buried bit lines in said substrate arranged substantially parallel to one another and arranged to connect memory cells in the same column; each first buried bit line electrically connected to the first

terminal of memory cells arranged in the same column; wherein adjacent memory cells in the same row share a common first terminal; said first terminal being along the bottom wall of said first trench; each second buried bit line electrically connected to the second terminal of memory cells arranged in the same column, wherein adjacent memory cells in the same row share a common second terminal; said second terminal being along the bottom wall of said second trench; a plurality of gate lines arranged substantially parallel to one another, each gate line electrically connected to the transistor gate of memory cells arranged in the same column; and a plurality of word lines arranged substantively parallel to one another, each word line electrically connected to the first and second control gates of each memory cell arranged in the same row; wherein first floating gates of first memory cells in the same column are positioned in the same trench insulated from said first sidewall, and first floating gates of second memory cells in the same column, adjacent to said first memory cells are positioned in said same trench insulated from said second sidewall; said method comprising;

applying a first voltage to a first buried bit line connecting to the first terminal of the selected memory cell;

applying a second voltage, more positive than said first voltage, to a second buried bit line connecting to the second terminal of the selected memory cell;

applying a third positive voltage to the word line connecting the first and second control gates of the selected memory cell; said third positive voltage sufficient to turn on the first and third portions of the channel of the selected memory cell irrespective of the amount of charges stored thereon; and

applying a fourth positive voltage to the gate line connecting to the transistor gate of the selected memory cell; said fourth positive voltage sufficient to turn on the second portion of the channel;

whereby charges from said first terminal are injected onto the second floating gate of the selected memory cell to program said second floating gate.

52. The method of claim 51 wherein said fourth positive voltage for controlling the amount of charges from said first terminal are injected onto said second floating gate.

53. The method of claim 51 wherein said first voltage is ground.

54. The method of claim 51 further comprising:

applying a fifth voltage to the gate lines not connecting to the transistor gate of the selected memory cell; said fifth voltage insufficient to turn on the second portion of said channel of the unselected memory cells.

55. The method of claim 54 wherein said fifth voltage is ground

56. The method of claim 54 further comprising:

applying a sixth voltage to the word lines not connecting to the control gates of the selected memory cell; said sixth voltage insufficient to turn on the first and third portions of the channel of the unselected memory cells.

57. The method of claim 56 wherein said sixth voltage is ground.

58. The method of claim 54 further comprising:

applying a seventh voltage to the buried bit lines not connecting to the selected memory cell; said seventh voltage is on the order of said first voltage.

59. The method of claim 58 wherein said seventh voltage is ground.

60. A method of making an isolation-less array of non-volatile memory cells in a semiconductor substrate of a first conductively type comprising;

forming a plurality of spaced apart trenches in said substrate in a first direction, each trench having a first sidewall, a second sidewall and a bottom wall;

forming a first terminal of a second conductivity type along the bottom wall of each trench in the substrate;

forming a pair of floating gates along the first and second sidewalls in each trench, each floating gate spaced apart from the first and second sidewalls, respectively;

forming a control gate in each trench; each control gate insulated from and

capacitively coupled to the floating gates in the trench and insulated from the first terminal along the bottom wall of the trench;

patterning said substrate along a second direction substantially perpendicular to said first direction and forming a plurality of spaced apart insulation regions in each trench and forming a plurality of floating gates in said first direction insulated from one another;

forming a plurality of spaced apart, substantially parallel, transistor gates, each transistor gate extending in said first direction and spaced apart and insulated from the substrate, and positioned adjacent to a trench in a region between each pair of trenches; and

forming an electrical contact to each control gate in the same second direction.

61. A method of making an isolation-less array of non-volatile memory cells in a semiconductor substrate of a first conductively type, comprising;

forming a plurality of spaced apart substantially parallel masked regions on said substrate in a first direction, wherein an unmasked region is formed on said substrate between each pair of adjacent masked regions;

forming a pair of spaced apart transistor gates substantially parallel to one another extending in said first direction in each unmasked region, with each transistor gate adjacent to a masked region, spaced apart and insulated from the substrate;

removing said masked regions;

forming a trench region in said substrate extending in said first direction, between each pair of adjacent unmasked regions; each trench having a first sidewall, a second sidewall, and a bottom wall;

forming a first terminal of a second conductively type in the substrate extending in said first direction, along the bottom wall of each trench;

forming a pair of floating gates along the first and second sidewalls, respectively, in each trench, each floating gate spaced apart from its respective sidewall;

forming a control gate in each trench; each control gate insulated from and capacitively coupled to the floating gates in the trench and insulated from the second terminal along the bottom wall of each trench;

patterning each trench along a second direction substantially perpendicular to said

first direction and forming a plurality of spaced apart insulation regions in each trench; and

forming an electrical contact to each control gate that are positioned in the same second direction.

62. A method of making an isolation-less array of non-volatile memory cells in a semiconductor substrate of a first conductively type, comprising;

forming a plurality of spaced apart substantially parallel masked regions on said substrate in a first direction, wherein an unmasked region is formed on said substrate between each pair of adjacent masked regions;

forming a plurality of buried bit lines in said substrate, with each buried bit line in each unmasked region, substantially parallel to one another extending in said first direction;

forming a plurality of floating gates, with each floating gate insulated from each buried bit line in said unmasked region; each floating substantially parallel to one another extending in said first direction;

forming a plurality of control gates, with each control gate insulated from each floating gate and capacitively coupled thereto in said unmasked region; each control gate substantially parallel to one another extending in said first direction;

removing said masked regions;

forming a trench region in said substrate extending in said first direction, between each pair of adjacent unmasked regions; each trench region having a side wall and a bottom wall;

forming a gate electrode in each trench; each gate electrode insulated from said side wall and said bottom wall of each trench; each gate electrode substantially parallel to one another extending in said first direction

patterning each control gate along a second direction substantially perpendicular to said first direction to cut through said control gate and floating gate forming a plurality of spaced apart insulation regions in each first direction; and

forming an electrical contact to each control gate that are positioned in the same second direction.